WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device having a write operation mode, a read operation mode, and an erase operation mode, the nonvolatile semiconductor memory device comprising:

a memory cell array in which a plurality of nonvolatile semiconductor memory cells in which data is electrically erased/written are arranged in a matrix, some of the plurality of memory cells form a normal memory cell group including a normal memory space, remaining memory cells among the plurality of memory cells form a redundancy memory cell group including a redundancy memory space, the plurality of memory cells are divided into a plurality of cell blocks for each unit by which stored data is electrically collectively erased, and the plurality of memory cells in each cell block are formed in a plurality of semiconductor regions electrically isolated from each other;

a plurality of normal word lines which are disposed in the respective cell blocks and which are connected to the memory cells in the normal memory cell group and which select the memory cells in the normal memory cell groups;

a plurality of redundancy word lines which are disposed in the respective cell blocks and which are connected to the memory cells in the redundancy memory cell group and which are replaced with the normal word

lines and used, and which select the memory cells in the redundancy memory cell group;

a plurality of bit lines which are disposed in the respective cell blocks and which are connected to the memory cells in the normal memory cell group and the memory cells in the redundancy memory cell group;

a well control circuit which is connected to the plurality of semiconductor regions and which applies a first voltage having a positive polarity to the semiconductor region corresponding to at least one cell block among the plurality of cell blocks, at the time of the erase operation mode; and

a row decoder which is connected to the plurality of cell blocks and which selects the plurality of cell blocks, the plurality of normal word lines, and the plurality of redundancy word lines and which supplies a second voltage having a negative polarity to the selected normal word line corresponding to a normal memory cell in the selected cell block at the time of the erase operation mode to control the erase operation of the memory cell and which supplies a third voltage having a potential difference from the first voltage is smaller than that between the first voltage and second voltage to the selected normal word line corresponding to a defective memory cell and the redundancy word line which has not been replaced.

2. A nonvolatile semiconductor memory device

according to claim 1, wherein the third voltage is lower than the first voltage and which has a positive polarity.

3. A nonvolatile semiconductor memory device according to claim 1, further comprising:

a defective address memory circuit in which a defective row address corresponding to a defective memory cell present in the plurality of cell blocks is stored;

a comparison circuit which is connected to the defective address memory circuit and which receives an external input address and the stored address of the defective address memory circuit and compares the addresses with each other to output a comparison result indicating agreement/disagreement;

an address multiplexer which is connected to the comparison circuit and which selects the stored address of the defective address memory circuit as an address for replacing the normal word line corresponding to the defective memory cell with the redundancy word line, when the comparison result indicates agreement, and which selects the external input address, when the comparison result indicates the disagreement and which outputs internal address signals; and

a column control circuit which is connected to the plurality of cell blocks and which controls a selection operation of the plurality of bit lines in each cell

block and which sets the selected bit line to a predetermined voltage state in accordance with the operation mode.

4. A nonvolatile semiconductor memory device according to claim 1, wherein each of the plurality of normal word lines and the plurality of redundancy word lines in the plurality of cell blocks includes a double word line structure.

5. A nonvolatile semiconductor memory device according to claim 3, wherein the row decoder includes:

a first row decoder circuit which is disposed in common with respect to the plurality of cell blocks and which outputs a first selection signal based on an upper row address signal included in the internal address signal;

a second decoder circuit which is disposed in common with respect to the plurality of cell blocks and which outputs a second selection signal based on a lower row address signal included in the internal address signal; and

a third row decoder circuit which is disposed for each of the plurality of cell blocks and which is connected to the first and second row decoder circuits and which selects the cell block based on the first and second selection signals and which further selects the plurality of normal word lines and redundancy word lines in the selected cell block and which supplies the

second voltage to the normal word line corresponding to the normal memory cell in the selected cell block or the replaced redundancy word line and supplies the third voltage to the normal word line corresponding to the defective memory cell and the redundancy word line which has not been replaced at the time of the erase operation mode of the selected cell block.

6. A nonvolatile semiconductor memory device according to claim 5, wherein the third row decoder circuit includes:

a plurality of first transfer gates each of which includes one end and the other end and one end each of which is connected to the plurality of normal word lines and redundancy word lines and in which one of the second and third voltage is supplied to the other end and which are selectively in an on state at the time of the write operation mode, the read operation mode, and the erase operation mode; and

a plurality of second transfer gates each of which includes one end and the other end and one end each of which is connected to a node of an erase bias voltage having the second voltage and the other end of which is connected to the plurality of normal word lines and redundancy word lines,

wherein the second voltage is supplied to the other end of the first transfer gate whose one end is connected to the normal word line corresponding to the

normal memory cell and the replaced redundancy word line, and the third voltage is supplied to the other end of the first transfer gate whose one end is connected to the normal word line corresponding to the defective memory cell or the redundancy word line which has not been replaced, at the time of the erase operation mode, and

the second transfer gate whose one end is connected to the normal word line corresponding to the normal memory cell and the replaced redundancy word line is controlled in on state to pass the second voltage, and the second transfer gate whose one end is connected to the normal word line corresponding to the defective memory cell and the redundancy word line which has not been replaced is controlled in off state, at the time of the block erase operation mode.

7. A nonvolatile semiconductor memory device according to claim 1, further comprising:

a self convergence control circuit which is connected to the plurality of cell blocks and which supplies a fourth voltage to all the word lines in the selected cell block and selects the plurality of bit lines in the cell block to supply a fifth voltage after the erase operation in the selected cell block to control threshold voltages of all the memory cells in the selected cell block in a certain range.

8. A nonvolatile semiconductor memory device

according to claim 7, wherein the fourth voltage is 0 V, and the fifth voltage is a voltage having the positive polarity between the second voltage and the first voltage.

9. A nonvolatile semiconductor memory device according to claim 1, wherein the plurality of memory cells arranged in the same column of the memory cell array is NOR connected.

10. A semiconductor integrated circuit device comprising:

a nonvolatile semiconductor memory circuit having a write operation mode, a read operation mode, and an erase operation mode, the nonvolatile semiconductor memory circuit is formed in a semiconductor chip, the nonvolatile semiconductor memory circuit including:

a memory cell array in which a plurality of nonvolatile semiconductor memory cells in which data is electrically erased/written are arranged in a matrix, some of the plurality of memory cells form a normal memory cell group including a normal memory space, remaining memory cells among the plurality of memory cells form a redundancy memory cell group including a redundancy memory space, the plurality of memory cells are divided into a plurality of cell blocks for each unit by which stored data is electrically collectively erased, and the plurality of memory cells in each cell block are formed in a plurality of semiconductor

regions electrically isolated from each other,

a plurality of normal word lines which are disposed in the respective cell blocks and which are connected to the memory cells in the normal memory cell group and which select the memory cells in the normal memory cell groups,

a plurality of redundancy word lines which are disposed in the respective cell blocks and which are connected to the memory cells in the redundancy memory cell group and which are replaced with the normal word lines and used and which select the memory cells in the redundancy memory cell group,

a plurality of bit lines which are disposed in the respective cell blocks and which are connected to the memory cells in the normal memory cell group and the memory cells in the redundancy memory cell group,

a well control circuit which is connected to the plurality of semiconductor regions and which applies a first voltage having a positive polarity to the semiconductor region corresponding to at least one selected cell block among the plurality of cell blocks at the time of the erase operation mode, and

a row decoder which is connected to the plurality of cell blocks and which selects the plurality of cell blocks, the plurality of normal word lines, and the plurality of redundancy word lines and which supplies a second voltage having a negative

polarity to the selected normal word line corresponding to a normal memory cell in the selected cell block at the time of the erase operation mode to control the erase operation of the memory cell and which supplies a third voltage having a potential difference from the first voltage is smaller than that between the first voltage and second voltage to the selected normal word line corresponding to a defective memory cell and the redundancy word line which has not been replaced; and

a controller which is formed in the chip to control the nonvolatile semiconductor memory circuit.

11. An electronic card comprising:

a semiconductor chip in which a nonvolatile semiconductor memory circuit having a write operation mode, a read operation mode, and an erase operation mode is formed, the nonvolatile semiconductor memory circuit including:

a memory cell array in which a plurality of nonvolatile semiconductor memory cells in which data is electrically erased/written are arranged in a matrix, some of the plurality of memory cells form a normal memory cell group including a normal memory space, remaining memory cells among the plurality of memory cells form a redundancy memory cell group including a redundancy memory space, the plurality of memory cells are divided into a plurality of cell blocks for each unit by which stored data is electrically collectively

erased, and the plurality of memory cells in each cell block are formed in a plurality of semiconductor regions electrically isolated from each other,

a plurality of normal word lines which are disposed in the respective cell blocks and which are connected to the memory cells in the normal memory cell group and which select the memory cells in the normal memory cell groups,

a plurality of redundancy word lines which are disposed in the respective cell blocks and which are connected to the memory cells in the redundancy memory cell group and which are replaced with the normal word lines and used, and which select the memory cells in the redundancy memory cell group,

a plurality of bit lines which are disposed in the respective cell blocks and which are connected to the memory cells in the normal memory cell group and the memory cells in the redundancy memory cell group,

a well control circuit which is connected to the plurality of semiconductor regions and which applies a first voltage having a positive polarity to the semiconductor region corresponding to at least one selected cell block among the plurality of cell blocks at the time of the erase operation mode, and

a row decoder which is connected to the plurality of cell blocks and which selects the plurality of cell blocks, the plurality of normal word

lines, and the plurality of redundancy word lines, and which supplies a second voltage having a negative polarity to the selected normal word line corresponding to a normal memory cell in the selected cell block at the time of the erase operation mode to control the erase operation of the memory cell and which supplies a third voltage having a potential difference from the first voltage is smaller than that between the first voltage and second voltage to the selected normal word line corresponding to a defective memory cell or the redundancy word line which has not been replaced; and

a card in which the semiconductor chip is incorporated.

12. An electronic apparatus comprising:

an electronic card including a semiconductor chip in which a nonvolatile semiconductor memory circuit is formed and a package in which the semiconductor chip is sealed, the nonvolatile semiconductor memory circuit having a write operation mode, a read operation mode, and an erase operation mode, the nonvolatile semiconductor memory circuit including:

a memory cell array in which a plurality of nonvolatile semiconductor memory cells in which data is electrically erased/written are arranged in a matrix, some of the plurality of memory cells form a normal memory cell group including a normal memory space, remaining memory cells among the plurality of memory

cells form a redundancy memory cell group including a redundancy memory space, the plurality of memory cells are divided into a plurality of cell blocks for each unit by which stored data is electrically collectively erased, and the plurality of memory cells in each cell block are formed in a plurality of semiconductor regions electrically isolated from each other,

a plurality of normal word lines which are disposed in the respective cell blocks and which are connected to the memory cells in the normal memory cell group and which select the memory cells in the normal memory cell groups,

a plurality of redundancy word lines which are disposed in the respective cell blocks and which are connected to the memory cells in the redundancy memory cell group and which are replaced with the normal word lines and used, and which select the memory cells in the redundancy memory cell group,

a plurality of bit lines which are disposed in the respective cell blocks and which are connected to the memory cells in the normal memory cell group and the memory cells in the redundancy memory cell group,

a well control circuit which is connected to the plurality of semiconductor regions and which applies a first voltage having a positive polarity to the semiconductor region corresponding to at least one cell block among the plurality of cell blocks at the

time of the erase operation mode, and

a row decoder which is connected to the plurality of cell blocks and which selects the plurality of cell blocks, the plurality of normal word lines, and the plurality of redundancy word lines and which supplies a second voltage having a negative polarity to the selected normal word line corresponding to a normal memory cell in the selected cell block at the time of the erase operation mode to control the erase operation of the memory cell and which supplies a third voltage having a potential difference from the first voltage is smaller than that between the first voltage and second voltage to the selected normal word line corresponding to a defective memory cell and the redundancy word line which has not been replaced;

a card slot electrically connected to the electronic card; and

a card interface connected to the card slot.

13. A digital still camera comprising:

an electronic card including a semiconductor chip in which a nonvolatile semiconductor memory circuit is formed and a package in which the semiconductor chip is sealed, the nonvolatile semiconductor memory circuit having a write operation mode, a read operation mode, and an erase operation mode, the nonvolatile semiconductor memory circuit including:

a memory cell array in which a plurality of

nonvolatile semiconductor memory cells in which data is electrically erased/written are arranged in a matrix, some of the plurality of memory cells form a normal memory cell group including a normal memory space, remaining memory cells among the plurality of memory cells form a redundancy memory cell group including a redundancy memory space, the plurality of memory cells are divided into a plurality of cell blocks for each unit by which stored data is electrically collectively erased, and the plurality of memory cells in each cell block are formed in a plurality of semiconductor regions electrically isolated from each other,

a plurality of normal word lines which are disposed in the respective cell blocks and which are connected to the memory cells in the normal memory cell group and which select the memory cells in the normal memory cell groups,

a plurality of redundancy word lines which are disposed in the respective cell blocks and which are connected to the memory cells in the redundancy memory cell group and which are replaced with the normal word lines and used, and which select the memory cells in the redundancy memory cell group,

a plurality of bit lines which are disposed in the respective cell blocks and which are connected to the memory cells in the normal memory cell group and the memory cells in the redundancy memory cell group,

a well control circuit which is connected to the plurality of semiconductor regions and which applies a first voltage having a positive polarity to the semiconductor region corresponding to at least one cell block among the plurality of cell blocks at the time of the erase operation mode, and

a row decoder which is connected to the plurality of cell blocks and which selects the plurality of cell blocks, the plurality of normal word lines, and the plurality of redundancy word lines and which supplies a second voltage having a negative polarity to the selected normal word line corresponding to a normal memory cell in the selected cell block at the time of the erase operation mode to control the erase operation of the memory cell and which supplies a third voltage having a potential difference from the first voltage is smaller than that between the first voltage and second voltage to the selected normal word line corresponding to a defective memory cell and the redundancy word line which has not been replaced;

a card slot electrically connected to the electronic card; and

a card interface connected to the card slot.

14. A personal digital assistant comprising:

an electronic card including a semiconductor chip in which a nonvolatile semiconductor memory circuit is formed and a package in which the semiconductor chip is

sealed, the nonvolatile semiconductor memory circuit having a write operation mode, a read operation mode, and an erase operation mode, the nonvolatile semiconductor memory circuit including:

a memory cell array in which a plurality of nonvolatile semiconductor memory cells in which data is electrically erased/written are arranged in a matrix, some of the plurality of memory cells form a normal memory cell group including a normal memory space, remaining memory cells among the plurality of memory cells form a redundancy memory cell group including a redundancy memory space, the plurality of memory cells are divided into a plurality of cell blocks for each unit by which stored data is electrically collectively erased, and the plurality of memory cells in each cell block are formed in a plurality of semiconductor regions electrically isolated from each other,

a plurality of normal word lines which are disposed in the respective cell blocks and which are connected to the memory cells in the normal memory cell group and which select the memory cells in the normal memory cell groups,

a plurality of redundancy word lines which are disposed in the respective cell blocks and which are connected to the memory cells in the redundancy memory cell group and which are replaced with the normal word lines and used, and which select the memory

cells in the redundancy memory cell group,

a plurality of bit lines which are disposed in the respective cell blocks and which are connected to the memory cells in the normal memory cell group and the memory cells in the redundancy memory cell group,

a well control circuit which is connected to the plurality of semiconductor regions and which applies a first voltage having a positive polarity to the semiconductor region corresponding to at least one cell block among the plurality of cell blocks at the time of the erase operation mode, and

a row decoder which is connected to the plurality of cell blocks and which selects the plurality of cell blocks, the plurality of normal word lines, and the plurality of redundancy word lines and which supplies a second voltage having a negative polarity to the selected normal word line corresponding to a normal memory cell in the selected cell block at the time of the erase operation mode to control the erase operation of the memory cell and which supplies a third voltage having a potential difference from the first voltage is smaller than that between the first voltage and second voltage to the selected normal word line corresponding to a defective memory cell and the redundancy word line which has not been replaced;

a card slot electrically connected to the electronic card; and

a card interface connected to the card slot.

15. A voice recorder comprising:

an electronic card including a semiconductor chip in which a nonvolatile semiconductor memory circuit is formed and a package in which the semiconductor chip is sealed, the nonvolatile semiconductor memory circuit having a write operation mode, a read operation mode, and an erase operation mode, the nonvolatile semiconductor memory circuit including:

a memory cell array in which a plurality of nonvolatile semiconductor memory cells in which data is electrically erased/written are arranged in a matrix, some of the plurality of memory cells form a normal memory cell group including a normal memory space, remaining memory cells among the plurality of memory cells form a redundancy memory cell group including a redundancy memory space, the plurality of memory cells are divided into a plurality of cell blocks for each unit by which stored data is electrically collectively erased, and the plurality of memory cells in each cell block are formed in a plurality of semiconductor regions electrically isolated from each other,

a plurality of normal word lines which are disposed in the respective cell blocks and which are connected to the memory cells in the normal memory cell group and which select the memory cells in the normal memory cell groups,

a plurality of redundancy word lines which are disposed in the respective cell blocks and which are connected to the memory cells in the redundancy memory cell group and which are replaced with the normal word lines and used, and which select the memory cells in the redundancy memory cell group,

a plurality of bit lines which are disposed in the respective cell blocks and which are connected to the memory cells in the normal memory cell group and the memory cells in the redundancy memory cell group,

a well control circuit which is connected to the plurality of semiconductor regions and which applies a first voltage having a positive polarity to the semiconductor region corresponding to at least one cell block among the plurality of cell blocks at the time of the erase operation mode, and

a row decoder which is connected to the plurality of cell blocks and which selects the plurality of cell blocks, the plurality of normal word lines, and the plurality of redundancy word lines and which supplies a second voltage having a negative polarity to the selected normal word line corresponding to a normal memory cell in the selected cell block at the time of the erase operation mode to control the erase operation of the memory cell and which supplies a third voltage having a potential difference from the first voltage is smaller than that between the first

voltage and second voltage to the selected normal word line corresponding to a defective memory cell and the redundancy word line which has not been replaced;

a card slot electrically connected to the electronic card; and

a card interface connected to the card slot.

16. A PC card comprising:

an electronic card including a semiconductor chip in which a nonvolatile semiconductor memory circuit is formed and a package in which the semiconductor chip is sealed, the nonvolatile semiconductor memory circuit having a write operation mode, a read operation mode, and an erase operation mode, the nonvolatile semiconductor memory circuit including:

a memory cell array in which a plurality of nonvolatile semiconductor memory cells in which data is electrically erased/written are arranged in a matrix, some of the plurality of memory cells form a normal memory cell group including a normal memory space, remaining memory cells among the plurality of memory cells form a redundancy memory cell group including a redundancy memory space, the plurality of memory cells are divided into a plurality of cell blocks for each unit by which stored data is electrically collectively erased, and the plurality of memory cells in each cell block are formed in a plurality of semiconductor regions electrically isolated from each other,

a plurality of normal word lines which are disposed in the respective cell blocks and which are connected to the memory cells in the normal memory cell group and which select the memory cells in the normal memory cell groups,

a plurality of redundancy word lines which are disposed in the respective cell blocks and which are connected to the memory cells in the redundancy memory cell group and which are replaced with the normal word lines and used, and which select the memory cells in the redundancy memory cell group,

a plurality of bit lines which are disposed in the respective cell blocks and which are connected to the memory cells in the normal memory cell group and the memory cells in the redundancy memory cell group,

a well control circuit which is connected to the plurality of semiconductor regions and which applies a first voltage having a positive polarity to the semiconductor region corresponding to at least one cell block among the plurality of cell blocks at the time of the erase operation mode, and

a row decoder which is connected to the plurality of cell blocks and which selects the plurality of cell blocks, the plurality of normal word lines, and the plurality of redundancy word lines and which supplies a second voltage having a negative polarity to the selected normal word line corresponding

to a normal memory cell in the selected cell block at the time of the erase operation mode to control the erase operation of the memory cell and which supplies a third voltage having a potential difference from the first voltage is smaller than that between the first voltage and second voltage to the selected normal word line corresponding to a defective memory cell and the redundancy word line which has not been replaced;

a card slot electrically connected to the electronic card; and

a card interface connected to the card slot.